REMARKS/ARGUMENTS

In its current state, this application includes claims 1 - 7, as amended following a Response to a first Office Action. The present Office Action has been deemed final by the Examiner. This Response, including the claim amendments and remarks set forth herein, is being submitted with a Request for Continued Examination. Accordingly, this document is in Response to the Final Office Action dated August 25, 2005. Applicants request reconsideration by the Examiner, based on this responsive document.

In the Office Action, the Examiner has rejected claim 7 under 35 U.S.C. §102(b) as being anticipated by Laing, et al., 5,399,975. Claims 1 - 6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Gabele, et al., 5,991,521 in view of Laing, et al. Applicants respectfully traverse the rejections, based on the amendments herein and the following remarks.

Applicants respectfully traverse the rejection of claim 7 as being anticipated by Laing, et al.

The Laing, et al. patent discloses a method of testing electrical conductivity of a connection between an integrated circuit device and a circuit board to which the device is connected. The method includes steps which include the application of a potential of a first amount to a connection, and the application of a potential of a second differing amount to the connection. A probe is then positioned adjacent the device, so as to sense current indirectly in the current path. The presence of the current indicates that the connection being tested is conductive.

Applicants respectfully submit that Laing, et al. do not teach or suggest Applicants' invention as defined in claim 7 as amended. Applicants' invention is not directed to detecting or otherwise testing connection continuity. Instead, Applicants' invention as defined in claim 7 is directed to a method for "restoring" faulty elements internal to the integrated circuit device. That is, the application of a voltage signal of a predefined level to the external connecting pin defined in

claim 7 produces a restoration of appropriate operation of the integrated circuit device. This is not a situation which involves a method for detecting faults. Instead, claim 7 assumes that a fault has been detected prior to application of the voltage signal to the external connecting pin. Applicants have found, as what can be characterized as surprising results, that the application of the voltage signal actually restores proper operation of the circuit device.

Applicants fully realize that the reasons set forth in the foregoing paragraph as to why Laing, et al. do not anticipate Applicants' invention as defined in claim 7 have been set forth in substantial part in response to the first Office Action. Applicants also fully understand that the Examiner did not consider these arguments to be persuasive. However, Applicants again respectfully submit that the Laing, et al. reference is not directed in any manner to "restoration" of faulty connections or faulty elements. Instead, it only describes a means for determining continuity between a connection on an integrated circuit and a connection to a printed circuit board. In no manner does this patent reference teach or suggest (or even mention) the concepts invented by the Applicants of the present application, namely that application of a voltage signal may be utilized to restore faulty connections between connecting pins and memory circuit elements. In this regard, and so as to further clarify Applicants' invention as defined in claim 7, claim 7 has been amended so as to define the method as further including restoration of a faulty connection between the external connecting pin and elements of the integrated circuit device as a result of the application of the voltage signal. Further, claim 7 has been amended to make clear that such restoration will occur only subject to the condition that the external connecting pin is not completely disconnected from the elements of the integrated circuit device. Applicants respectfully submit that this clarification to Applicants' invention as defined in claim 7 makes clear the distinctions between Applicants' invention and the teachings and suggestions of Laing, et al. Applicants' invention as defined in claim 7 is directed to "restoration" of faulty connections, where such faults do not consist of complete, physical disconnections. In contrast, Laing, et al. is only directed to "testing" for

continuity. Further, Laing, et al. is specifically directed to testing electrical continuity of a connection between an integrated circuit device and a circuit board to which the device is connected. For all of these reasons, Applicants respectfully submit that Applicants' invention as defined in claim 7 as amended is not anticipated by Laing, et al.

Applicants respectfully traverse the rejection of claim 1 - 6 as being unpatentable over Gabele, et al. in view of Laing, et al.

The Gabele, et al. patent discloses a method and system for checking for open circuit connections within an integrated circuit design. The design is represented by a hierarchical data structure.

Applicants respectfully traverse the alleged combination of Gabele, et al. and Laing, et al. Applicants submit that there is no teaching or suggestion in Gabele, et al. to apply voltage signals to certain of the connecting pins. Further, Laing, et al. neither teach nor suggest the use of their method of testing continuity of a connection to a configuration such as Gabele, et al. For these reasons, Applicants respectfully submit that Gabele, et al. and Laing, et al. can not be tenably combined.

Assuming, arguendo, that Gabele, et al. and Laing, et al. can be tenably combined, Applicants respectfully submit that the alleged combination still does not teach or suggest Applicants' invention as defined in claim 1 - 6 as amended. As earlier stated, Applicants' method as defined in claim 1 is a method for "restoring" a faulty connection within an integrated circuit device. The method does not, in any manner, only detect a faulty connection. It is the application of the voltage signal (to the connecting pins which appear to have a fault) for purposes of restoring the faulty connection which is a novel and nonobvious concept embodied within Applicants' invention.

In contrast, neither Gabele, et al. nor Laing, et al., taken either singularly or in an alleged combination, restore faulty connections by application of voltage signals to certain

connecting pins. For these reasons, Applicants respectfully submit that the alleged combination of Gabele, et al. and Laing, et al. does not teach or suggest Applicants' invention as defined in claim 1 as amended.

Applicants understand that a number of the arguments set forth in the foregoing paragraphs with respect to the patentability of claims 1 - 6 were earlier set forth in the response to the first Office Action. Applicants also understand that the Examiner fully considered these arguments, but did not deem them to be persuasive.

To further clarify Applicants' invention, Applicants have amended claim 1 so as to more specifically define the concept that the application of the voltage signal is not for purposes of testing, but instead is for purposes of restoration of faulty connections. In this regard, Applicants have first amended claim 1 so as to define the concept that connecting the voltage supply to certain of the connecting pins appearing to be disconnected is undertaken subsequent in time to obtaining the error message. In this regard, it is the process of obtaining the error message which more specifically corresponds to the activities identified as being undertaken by Gabele, et al. and Laing, et al. Further, claim 1 has been amended so as to more specifically define the concept that the method includes restoring faulty connections between the memory circuit element and at least one of the connecting pins appearing to be disconnected from the memory circuit element. That is, it is the application of the voltage signal itself which operates so as to restore the faulty connections. Once it has been determined that a faulty connection may exist, the functions described in Gabele, et al. and Laing, et al. have no further purpose. That is, the functions defined in these two references are directed solely to the concept of determining if any faulty connections exist with respect to testing of continuity. The novel concepts of Applicants' invention reside in functional steps undertaken following a determination that continuity appears to be absent or otherwise reduced. Again, with respect to Laing, et al., the functional steps taught or otherwise suggested by Laing are solely directed to the testing for continuity. In contrast, Applicants' application of the

voltage signal to certain of the connecting pins only occurs after the continuity test described in claim 1, and only occurs with respect to those connecting pins which appear to be disconnected (or partially disconnected) from the memory circuit element. For all of these reasons, Applicants respectfully request that the Examiner reconsider the rejection of claim 1 on the basis of the alleged combination.

Each of claims 2 - 6 is directly or indirectly dependent from claim 1, and is construed to include all limitations thereof. For the reasons set forth herein that claim 1 as amended is patentable over the alleged combination of Gabele, et al. and Laing, et al. Applicants respectfully submit that each of dependent claims 2 - 6 is also patentable over the alleged combination.

In view of the amendments to the claims and the remarks set forth herein, Applicants respectfully submit that each of claims 1 - 7, as amended, is now in condition for allowance, and early notification of allowability is respectfully requested. Should any questions arise in connection with the above, please contact Thomas L. Lockhart at the telephone number of 616/336-6000.

Respectfully submitted,

TIMOTHY CALVIN VISSER and GARY M. UHL

Dated: 2/24/2006

By _____

Thomas L. Lockhart, Reg. No. 29,324
VARNUM, RIDDERING, SCHMIDT & HOWLETT
Bridgewater Place
333 Bridge Street
Post Office Box 352
Grand Rapids, Michigan 49501-0352
(616) 336-6000

#1209459